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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,863	01/16/2004	Robert B. Staszewski	TI-35773	6568

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EXAMINER	
FLORES, LEON	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
05/06/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/758,863	**Applicant(s)** STASZEWSKI ET AL.	
	Examiner LEON FLORES	**Art Unit** 2611	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 23 April 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires *3* months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☒ Applicant's reply has overcome the following rejection(s): 25-26.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: *44-46*.
   Claim(s) objected to: *10,25 and 26*.
   Claim(s) rejected: *1-3,5-9,11-43 and 47-54*.
   Claim(s) withdrawn from consideration: *4*.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See continuation sheet.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/David C. Payne/
Supervisory Patent Examiner, Art Unit 2611

Applicant asserts that "A method for testing a radio frequency (RF) circuit" recited in the preamble is not taught or even suggested in Staszewski".

The examiner respectfully disagrees. In response to applicant's arguments, the recitation "testing" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Furthermore, a preamble that recites the use or purpose of the claimed invention generally does not limit the claims. See Catalina, 62 USPQ2d at 1785. However, taking the contrary, one skilled in the art would know that PLLs are first tested to see if they are working properly, and this is done prior to distribution.

Applicant further asserts that "The step of "observing a signal from the RF circuit" is not taught in Staszewski. Due to the lack of testing there, there is no motivation of doing so. The "signal", equated by Examiner to PHE in Fig. 4a is not suggested to be observed for the purpose of testing. The PHE signal is only fed to the gain circuit 70 as part of a normal ADPLL operation, which has nothing to do with testing. No other connections are shown, especially to the "outside of the RF circuit".

The examiner respectfully disagrees. First of all, the examiner has already addressed the issue of testing in the previous remark. And second of all, one skilled in the art would know that the signal of interest (the signal to be observed) in a PLL is the error signal. It is of real interest due to the fact that based on this error signal we can estimate if synchronization has been achieved and/or maintained.

Applicant further asserts that "The limitation of "wherein the signal has a high degree of correlation with an RF output of the RF circuit" is not taught or suggested in Staszewski. At the time of the reference patent publication, the ADPLL idea was still quite new and it would not have been known by one of average skill in the art that the PHE signal has a high degree of correlation with "an RF output,, such as output of the PA circuit".

The examiner respectfully disagrees. One skilled in the art would know that by filtering out frequencies components (frequency components not desired) which are above the cut off frequency of the loop filter, a high degree of correlation between the phase error (desired frequencies) and the RF output can be achieved. And this is b/c from the point that error signal passes the loop filter and reaches the output of the PA circuit there is no more filtering. This is notoriously well known in ADPLLs.

Applicant further asserts that ""one skilled in the art would know that by filtering out frequencies components (not desired) which are above the cut off frequency of the loop filter, a high degree correlation between the phase error (desired frequencies) and the RF output can be achieved - this is notoriously well known in ADPLLs (OA, page 3. lines 12-16)". Examiner's determination is not correct. While PLL filtering of external signals is well known, use of PLL filtering for "internal" signals, as required by the limitation "signal from within a processing portion of the RF circuit", is not known, in the event Examiner does not withdraw this determination, Applicants respectfully request that Examiner cite a reference to support this determination.

The examiner respectfully disagrees. The internal signal that applicant is referring to is the error signal. This error signal is generated within a PLL and it is the signal of interest. As previously stated, one skilled in the art would know that the signal of interest (the signal to be observed) within (internally) a PLL is the error signal. It is of real interest due to the fact that based on this error signal we can estimate if synchronization has been achieved and/or maintained.

Applicant further asserts that "Hence, the phase detector 10 output is not accessible nor is the PEP 12 output - making them available (despite various technical difficulties) would not provide any substantial benefits. As such, Examiner's determination is supposition not supported by fact -- little more than improper hindsight reconstruction".

1. The examiner respectfully disagrees. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See In re McLaughlin, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Applicant further asserts that "For the reasons set forth above, Wong, alone or in combination with Staszewski, does not teach or suggest "a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals", as required by Claim 1. The interface in Wong is asynchronous and there is simply no motivation to re-engineer the entire architecture which in itself is non- obvious to one of average skill in the art at the time of the invention, to allow synchronous signal controls of sufficient speed. For the reasons set forth above, the 35 U.S.C. 103(a) rejection of Claim 1 is improper and must be withdrawn".

The examiner respectfully disagrees. The examiner has no recollection that claim 1 recites "a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals". However, taking the contrary, the combination of Staszewski and Wong does teach/suggest "a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals" (In Wong, see figs. 1-2 & col. 1, line 38 – col. 2, line 3)

Applicant further asserts that ""all words in a claim must be considered in judging the patentability of that claim against the prior art, "In re Wilson. 424 F.2d 1382. 1385, 165 USPQ 494. 496 (CCPA 1970)".

The examiner agrees. However, the examiner would like to respectfully remind applicant that "claims must be "given their broadest reasonable interpretation consistent with the specification." >The Federal Circuit's en banc decision in Phillips v. AWH Corp., 415 F.3d 1303, 75 USPQ2d 1321 (Fed. Cir. 2005) expressly recognized that the USPTO employs the "broadest reasonable interpretation" standard. See MPEP 2111 [R-5].

Applicant further asserts that "Moreover, even had the Examiner considered all of the words of Claim 1, in proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior

art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Piasecki. 745 F.2d I468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984), "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing in re Fine. 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing in re Lalu, 747 F.2d 703, 705. 223 USPQ 1257, 1258 (Fed. Cir. 1988))".

The examiner respectfully disagrees. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both the references of Staszewski and Wong deal with PLLs.

Applicant further asserts that "Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in tile context of a purported obvious "modification" of the prior art-. The mere fact that the prior art may be modified in the manner suggested p by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Gordon. 733 F.2d at 902. 221 USPQ at 1127. Moreover. it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. In re Gorman, 933 F.2d 982. 987, 18 U SPQ2d 1885, 1888 (Fed.Cir. 1991). See also interconnect Planning Corp. y. Fell, 774 F.2d i132. Ii38, 227 USPQ 543. 547 (F d,Clr.198z)".

The examiner respectfully disagrees. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant further asserts that "Staszewski does not teach "wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation" limitation, as required by Claim 41".

The examiner agrees. However, the examiner did not use the reference of Staszewski to reject this limitation. The examiner, in the other hand, used the reference of Wong to reject this limitation.

Applicant further asserts that "to copy from the previous amendment: detector containing circuitry to compute a difference between the reference phase and a variable phase .... ". Wong only teaches UP/DOWN phase direction information, which is not the phase error estimation signal. There is no magnitude information, only the direction.">>. As such, Examiner's determination of the teaching of Wong is erroneous".

The examiner respectfully disagrees. The reference of Wong does teach that this signal is the phase error. (See fig. 2 & col. 2, lines 50-57 "phase error information") However, taking the contrary, applicant, at any point, claims that the signal must show magnitude information.

Applicant further asserts that "Applicants disagree with Examiner's contention that one skilled in the art "would know that if the loop filter is designed in such as way (adjusting filter's parameters) so that the frequency of the error signal is within the cutoff frequency of the loop filter, then a high degree of correlation can be achieved between the error signal and the output signal". Applicants respectfully request Examiner to provide evidence from the prior art supporting his assertion or withdraw the determination. Furthermore, when a high degree of correlation is achieved the transfer function wil1 be flat within a specific frequency range". At the time of the instant application, the knowledge that the digital PHE signal was highly correlated with the RF output phase, and their transfer function was flat, was not obvious".

The examiner respectfully disagrees. One skilled in the art would know that the transfer function of two signal having a high degree of correlation would be flat or constant. And this can be shown to be true mathematically. Is applicant trying to claim well known mathematical equations?

Applicant further asserts that "the text in Wong cited by Examiner does not teach "the method thriller comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth", as required by Claim 24. The text only mention setting of various programmability modes, NOT bandwidths: "°The loop filter also includes a loop configuration circuit which in response to the digital tester 4 programs and via the LCP 24 configures the loop type of the DUT 2. The DPLL, for example, provides for different for eight different types of loop configurations in a test mode (8 different combinations of close loop, open loop, and enable/disable proportional/integral a paths) as shown in Table 1. Furthermore, Applicants respectfully traverse Examiner's determination that. "Wong does teach "the loop filter also includes a loop configuration circuit for configuring the loop type of the DUT (see col. 3, lines 19-25 & table" 1)(OA, page 9, line 21 -page 10, line 1) ". Applicants respectfully respond that "loop type" is not a proper way of "setting the all-digital phase-locked loop to a certain bandwidth", Changing of loop type only introduces a pole at origin and does not control its bandwidth. At best, its effect would be parasitic or useless for a practical application. For the reasons set forth above, any combination of Staszewsld and Wong fails to teach or suggest all of the elements of Claim 24. The _35 U.S.C. 103(a) rejection is erroneous and must be withdrawn".

The examiner respectfully disagrees. The reference of Wong does teach "the loop filter also includes a loop configuration circuit for configuring the loop type of the DUT. (See col. 3, lines 19-26 & table 1) Furthermore, one skilled in the art would know that loop configuration is dependent on loop bandwidth. Furthermore, the loop bandwidth is dependent on what type of loop configuration the PLL will be operating.

Applicant further asserts that "Claim 25 further defines the method of claim 24, wherein the test is for estimating phase noise power and the signal is an output of a phase detector, and wherein the manipulating comprises calculating a mean square error of the signal. Claim 25 is allowable for the same reasons set forth above in support of the allowance of Claim 24. Moreover, the text identified by Examiner about recovered clock (RXC) jitter is irrelevant. It requires applying a "preconditioned input data pattern at the DPLL input (Din input on FIG 2)", which is not applicable in the present invention. The present- invention pertains to an ADPLL and a transmitter and does not concerns itself with the recovered clock. As such, any combination of Staszewski and Wong fails to teach or suggest a11 of the elements of Claim 25. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn,

The examiner agrees. The rejection to claim 25 has been withdrawn.

Applicant further asserts that “Claim 15 further defines the method of claim 14. wherein the phase error trajectory is good when the change in the signal is less than a specified threshold. Claim 15 is allowable for the same reasons set forth above in support of the allowance of Claim 14. Moreover none of the references pertain to the test ...for phase error trajectory". Further, the references, alone or in combination, do not teach the limitation of "wherein the manipulation comprises measuring a change in the signal". Examiner's statement, “the error signal is further compared with a threshold in order to determine if a coarse or fine adjustment is needed", is irrelevant as it does not pertain to "change in the signal” and testing in general”.
The examiner respectfully disagrees. One skilled in the art would know that the error signal is not a constant. It will change every time it is computed in the PLL. The reference of Girardeau does teach comparing the error signal with a threshold to see if there is any coarse or fine adjustment needed.

Applicant further asserts that “Applicants further traverse Examiner's new determination that "one skilled in the art would know that the phase error is the main signal of interest within a PLL (OA, page 11. lines 15-16)". Applicants respectfully submit that Examiner confuses "phase error trajectory" with “phase error". The two are different. Accordingly, for the reasons set forth above, any combination of Staszewski, Wong and Girardeau fails to teach or suggest all of the elements of Claim 15. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn”.
The examiner respectfully disagrees. The examiner is not confused with the phase error and the phase error trajectory. As previously stated, one skilled in the art would know that the error signal is not a constant. It will change every time it is computed in the PLL.

Applicant further asserts that “Kim's teaching of BIST is not applicable to the combination of Staszewski and Wong, Kim teaches the use of the traditional pulse-based phase detector and charge pump; It also requires the VCO divider. None of these circuits is used in Staszewski so Kim is not relevant here.
The examiner respectfully disagrees. In response to applicant's argument that Kim is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant’s endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the reference of Kim does use a BIST for testing PLLs

Applicant further asserts that “Wong's system is engineered in such as way as to minimize the data rate accessible through the I/O controller. Hence, the phase detector 10 output is not accessible nor is the PEP 12 output -making them available (despite various technical difficulties) would not provide rely substantial benefits. For the above reasons, Wong does not teach or suggest, "a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals." The interface in Wong is asynchronous and there is simply no motivation to re-engineer the entire architecture, which in itself is non-obvious to one of average skill in the art at the time of the invention, to allow synchronous signal controls of sufficient speed, as suggested by Examiner”.
The examiner respectfully disagrees. The examiner used the reference of Wong to reject the limitations of “a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals”. In claim 32 there is no limitation disclosing a phase detector. Furthermore, applicant is reminded that the claims limitations may be given its broadest reasonable interpretation.

Applicant finally asserts that “It does not teach performance testing associated with a cellular phone, nor does it even go beyond the PLL, which is merely a small building block of" a cell phone. Specifically he does not teach "performing built-in self test (B[ST) on a parameter associated with the cellular phone", as required by Claim 48”.
The examiner respectfully disagrees. The reference of Kim does teach performing built-in self test (B[ST) on a parameter associated with the cellular phone". (See col. 6, lines 9-49 “PLL”)